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Topological Array Trigger Review

System Overview

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June 20, 2008

U.S. Department
of Energy

UChicago
Argonne LLC

Office of
Science
U.S. DEPARTMENT OF ENERGY

A U.S. Department of Energy laboratory
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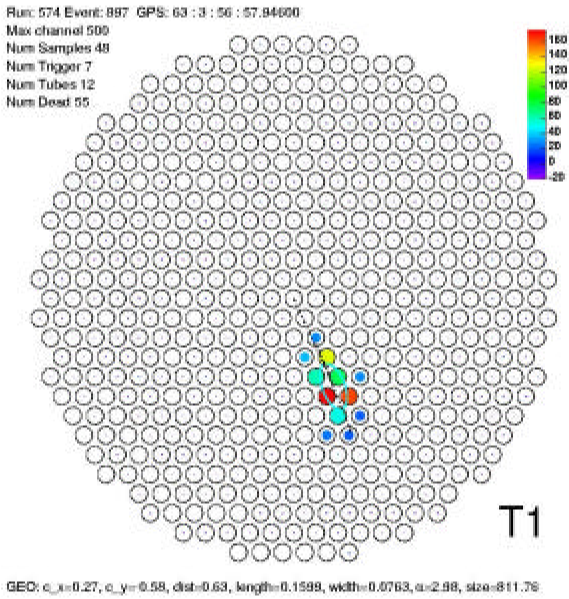
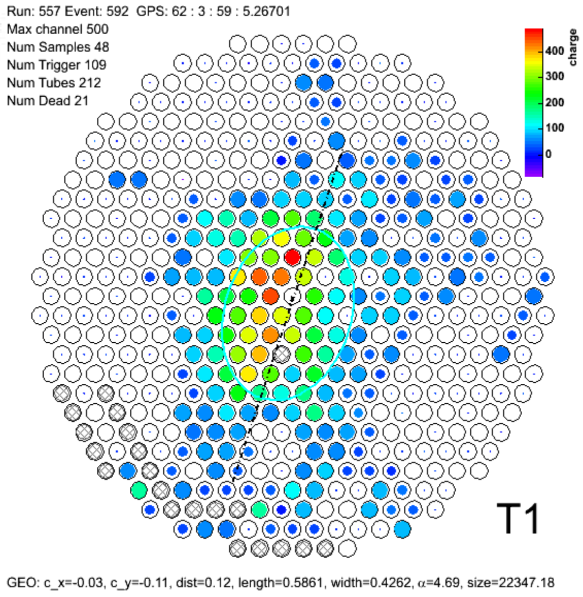
Basic Goal

- Develop and implement a real-time trigger to identify γ-ray events from other background events, as a basis for initiating DAQ readout

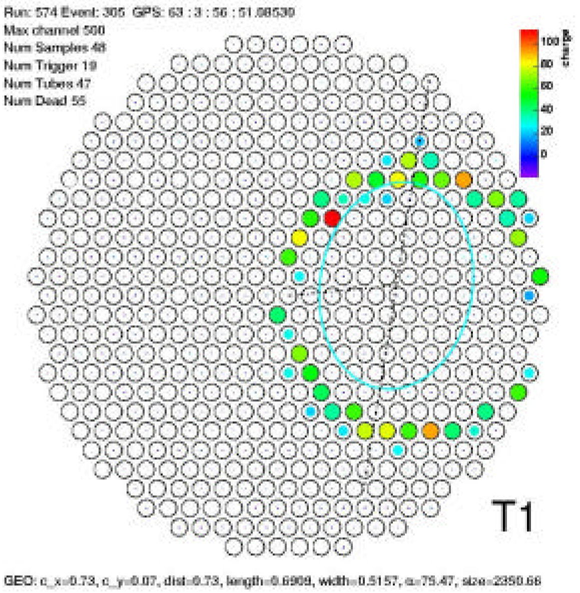
γ-ray Candidate



Cosmic Ray



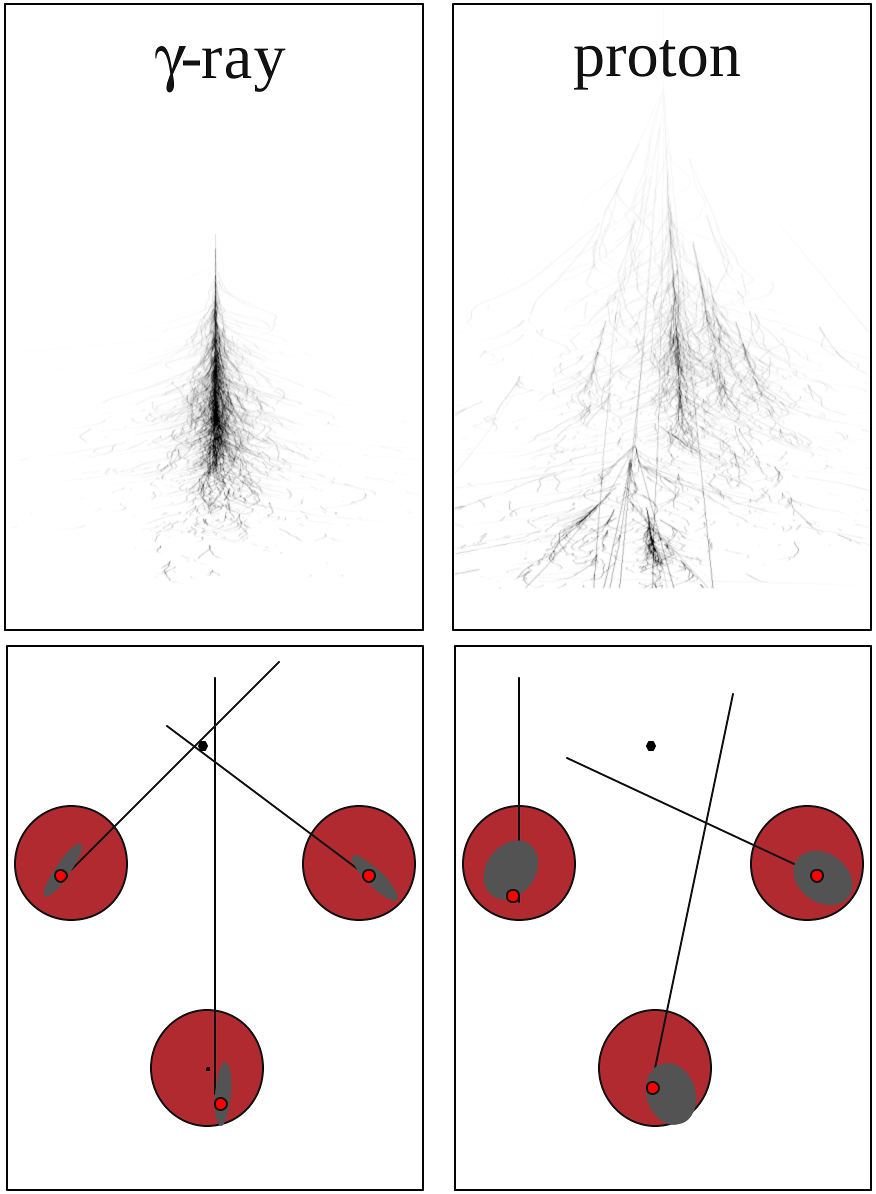
Muon



Veritas Telescope 1 Images Courtesy of Liz Hayes & Veritas

Basic Trigger Process

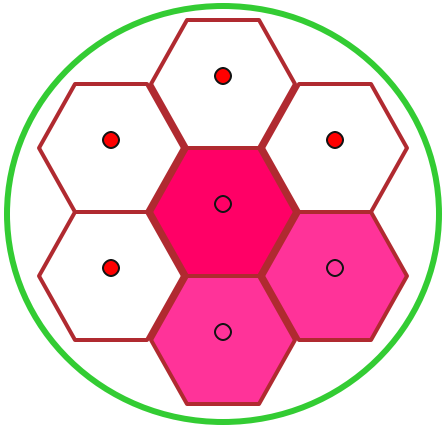
- Receive ***discriminated hits*** (Level 1 Trigger) of each pixel in a camera from the front-end electronics
- Form time window, & collect hits
- Calculate 1st & 2nd moments of images in each camera
- Use stereo view from multiple telescopes to project image back into the sky
- Identify γ-ray images by tight correlation of projection
- Do this in real-time:
  - ~10 MHz pixel rate → 5 GHz Camera rate (@ 500 Ch)
  - ~10 MHz L2 Output Rate
  - ~10 KHz L3 Output Rate

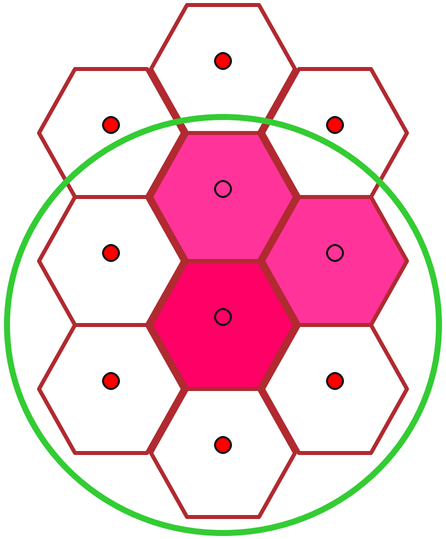


Graphic by F. Krennrich

Trigger Algorithm Basis

- Define configuration where each pixel has 6 neighbors (special cases for boundaries…)
- Basic processing:
  - Form time window, and look at pixel states
  - For each pixel, look to see if that pixel is hit
  - If yes, then next look to see if at least 2 neighbors are hit → ***3-fold coincidence***
  - If yes, then use X-Y coordinates for that pixel in further processing:
    - *Timestamp data*
    - *Collect X-Y coordinates of all hit pixels over entire camera*
    - *Calculate: n, Sx, Sy, Sx^2, Sy^2, Sxy*
    - *Send result of calculations to L3*
- Neighbor Logic Processing: ***400 MHz***

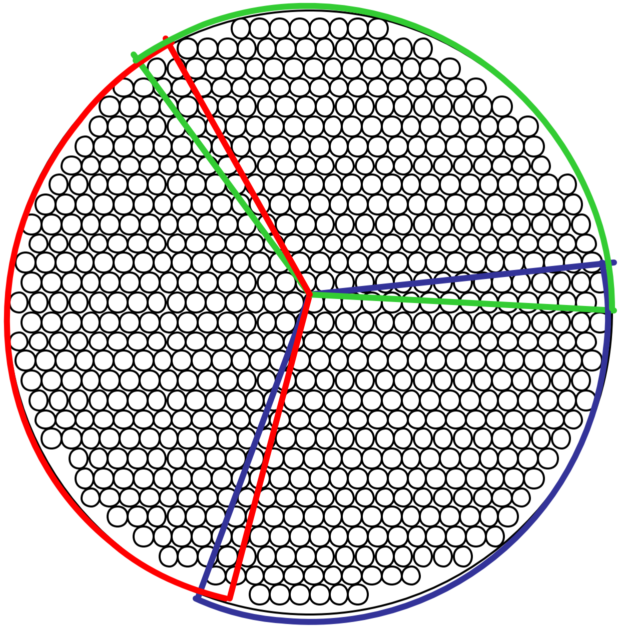




⇨ ***Has been demonstrated in Altera Stratix II***

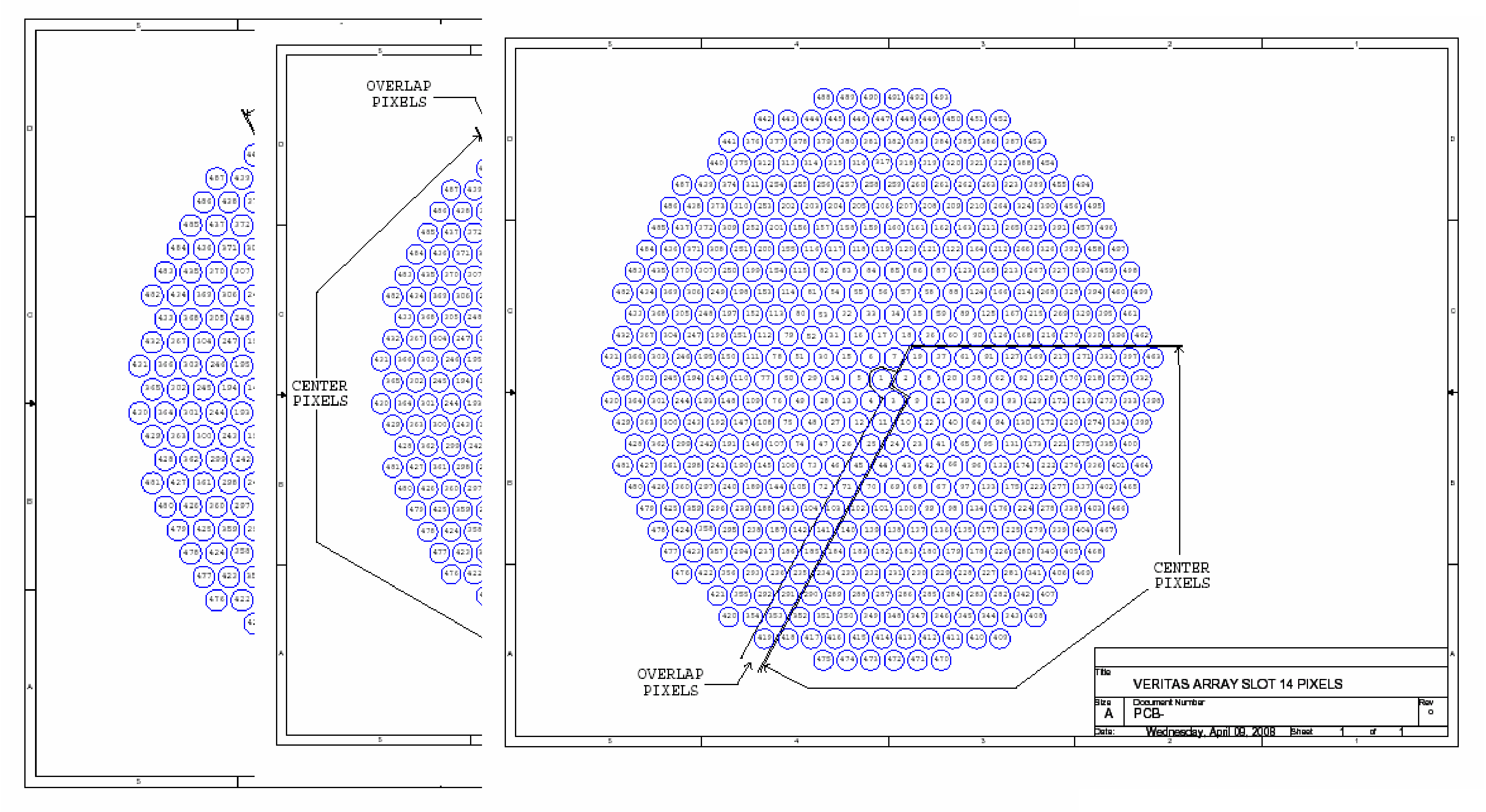
Physical Implementation

- 499 Pixels of Camera are Divided into ***3 Partitions***
  - Most pixels have “normal” neighbors – can form 7-pixel cells
  - Outer edges form cells with fewer than 7 pixels → special processing
  - 2 kinds of interior edges:
    - *Overlap region – uses pixels from neighboring partition to evaluate neighbor logic*
      → 1 pixel width is sufficient
    - *Non-overlap region – sends copy of pixel state to neighboring partition for evaluation*
- Processing will produce duplicates, which are discarded



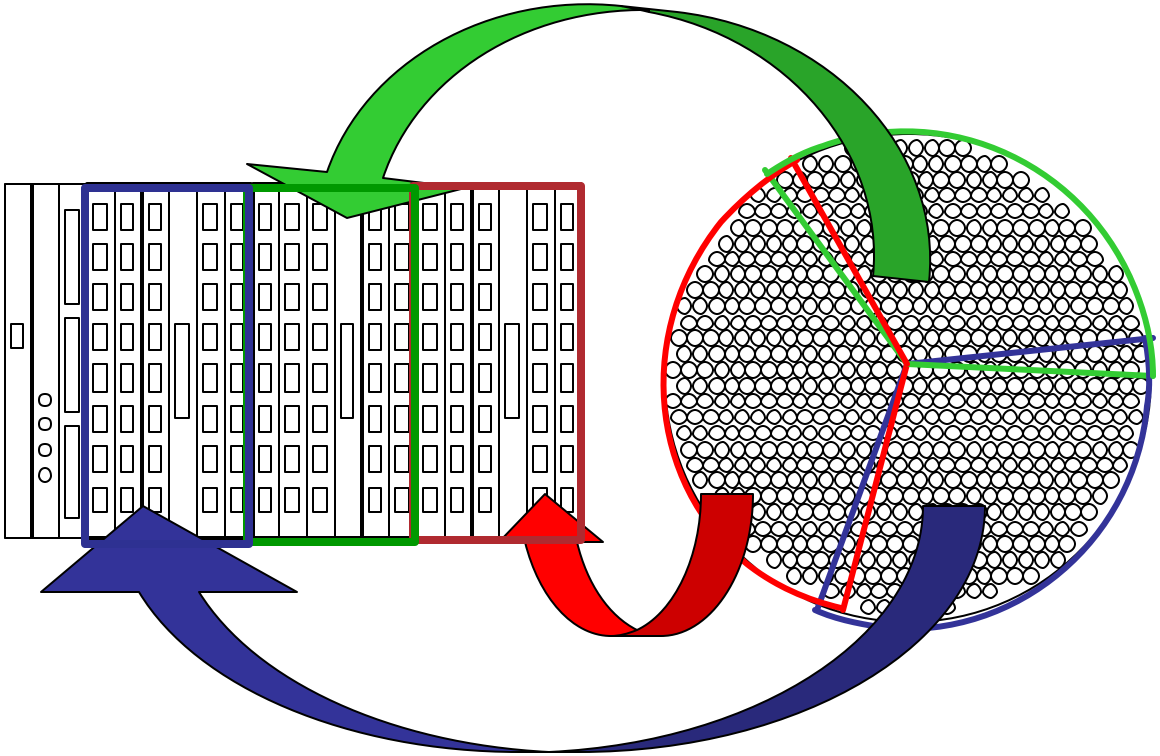
Physical Implementation

- Actual Partitions:



Physical Implementation (Cont.)

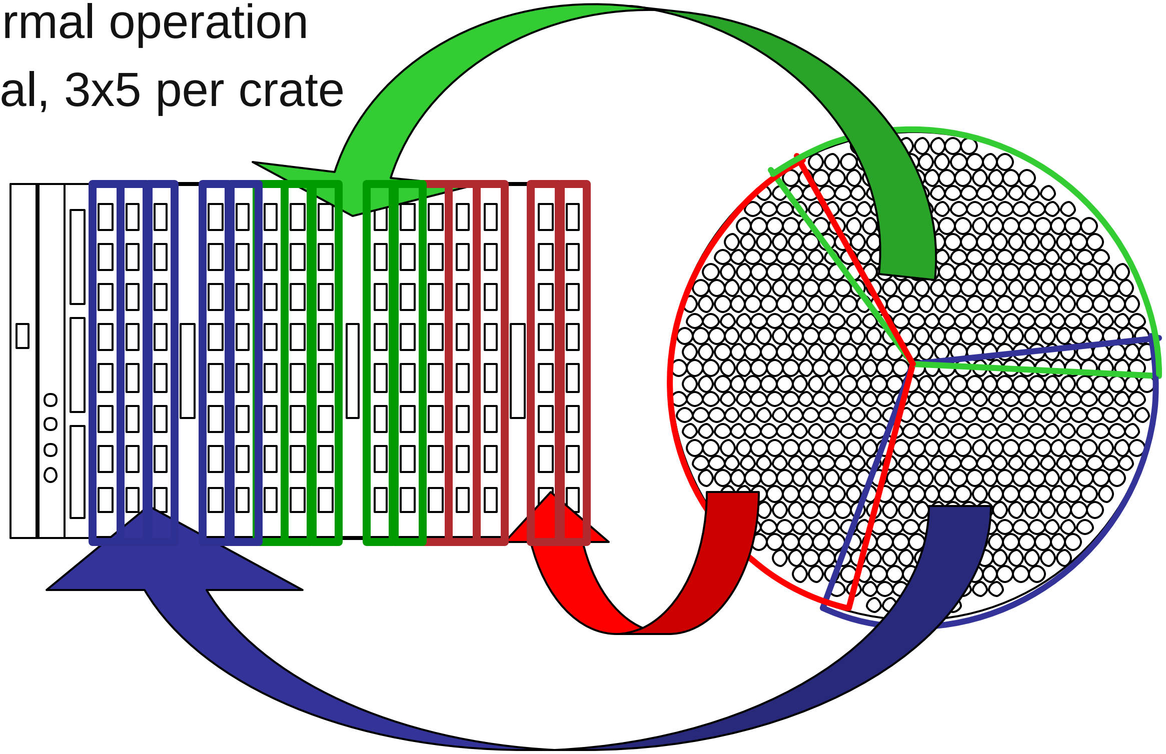
- "Level 2 Trigger" implemented in a 21-slot 9U Crate
  - Signals from each partition processed separately



Physical Implementation (Cont.)

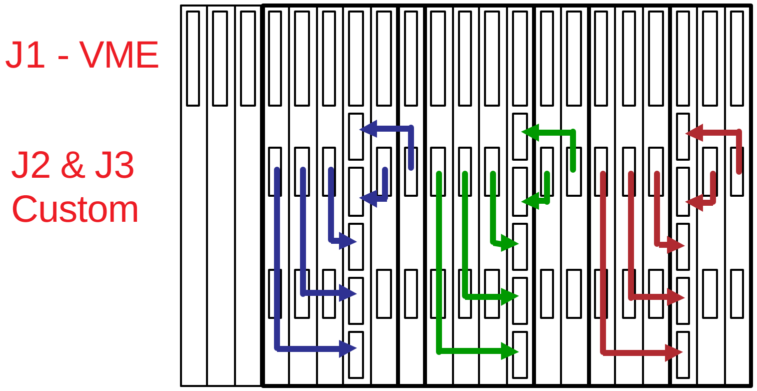
- I/O Cards
  - Receive L1 signals from front-end electronics (discriminated hits)
    - *Differential ECL, twisted-pair, 10 signal pairs per cable*
  - Copy (buffer) signals, & send across high-speed backplane to “L1.5 Processors” for processing → LVDS
  - ***Requirement:*** To test our demonstrator system in VERITAS, must not interfere with normal operation
  - All cards are identical, 3x5 per crate

⇨ *All signals come in and go out, with minimal signal degradation*



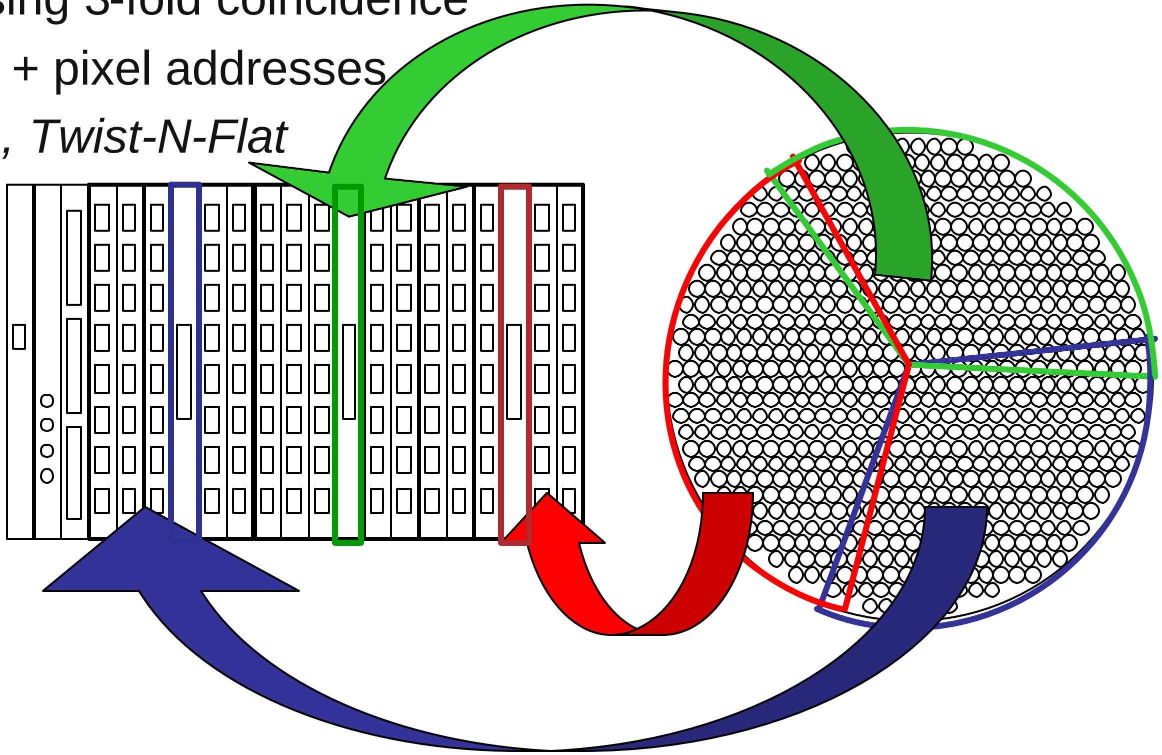
Physical Implementation (Cont.)

- Backplane
  - 9U Crate
  - J1: VME-64
  - J2 & J3: Full Custom
    - *Handles point-to-point routing of buffered L1 signals, from I/O Cards to L1.5 Processor*
    - *Routing is very specific, and assumes a definite connectivity architecture*
    - *Uses MultiGIG Connectors (Gbit/sec connectors)*
    - *2 connectors per I/O Card (1 for primary, 1 for overlap)*
    - *5 connectors per L1.5 Processor*
    - *Impedance matching, differential, lots of grounds*



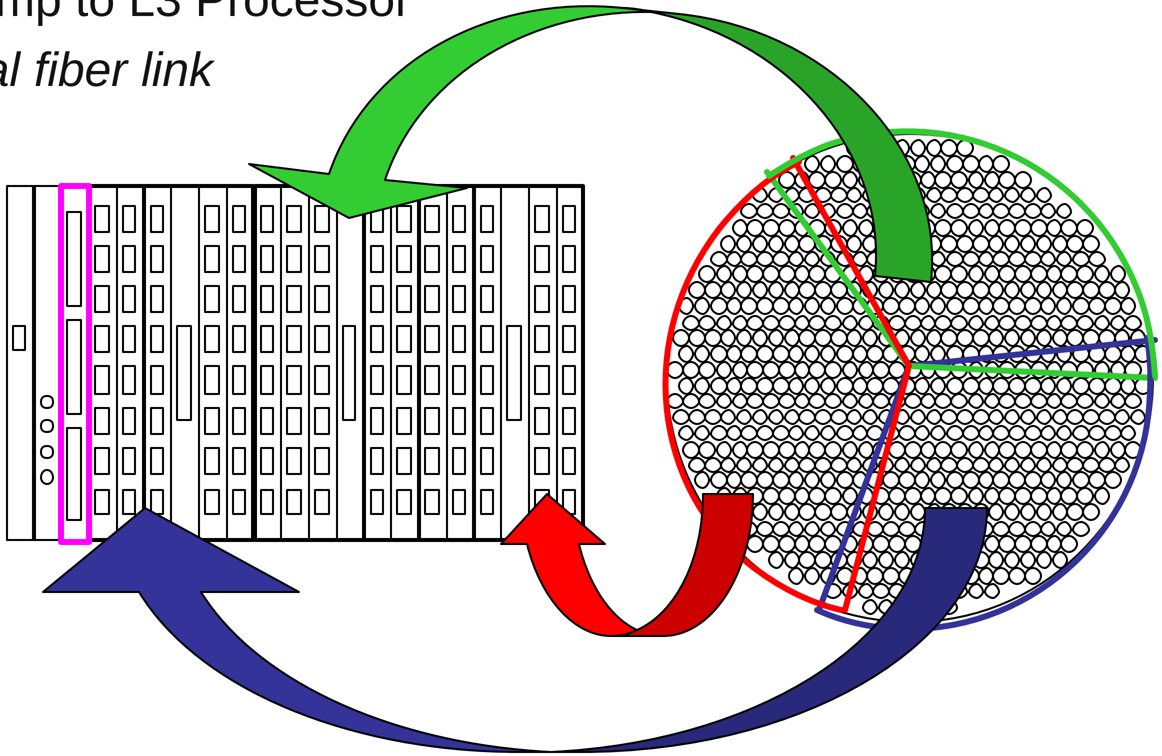
Physical Implementation (Cont.)

- Level 1.5 Processor
  - One L1.5 Processor per partition
  - Receive signals from I/O Cards in a given partition
    - *LVDS, ~166 pixels in each partition, ~13 overlap pixels*
  - Performs Neighbor Logic processing within programmable time window
  - Timestamp hits passing 3-fold coincidence
  - Output : Timestamp + pixel addresses
    - *LVDS, 16-bit data, Twist-N-Flat*
  - Send data to "L2 Processor"
  - Has VME Interface & diagnostics
  - All cards are identical, 3 per crate



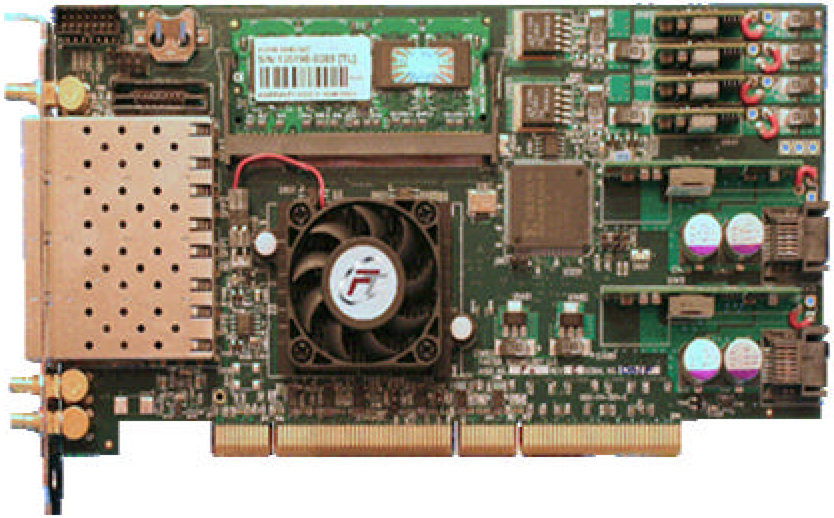
Physical Implementation (Cont.)

- Level 2 Processor
  - One L2 Processor per crate
  - Receives data from L1.5 Processors
  - Performs calculations on all pixels received from L1.5 Processors
  - Calculate: n, Sx, Sy, Sx^2, Sy^2, Sxy
  - Send data & timestamp to L3 Processor
    - *High-speed optical fiber link*
  - Other features:
    - *Clock tree*
    - *R/W comm. w/L3*
    - *VME access*
    - *Diagnostics*



Physical Implementation (Cont.)

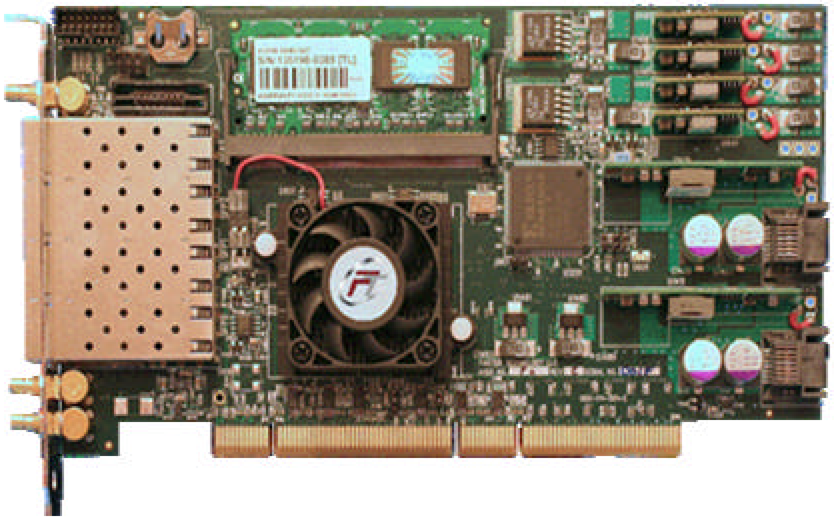
- Level 3 Processor
  - Receives 1st & 2nd moments from each L2 Crate, along with timestamps
  - Evaluates images, produces L3 Accept when criteria met
  - Uses timestamps to calculate hold-off time
  - Send L3 Accept to front ends at correct time



Faster Technology
P6 PCI FPGA Card

Physical Implementation (Cont.)

- Level 3 Processor
  - Current design: Commercial PCI card residing in a PC
  - Capable of interfacing to 4 L2 crates
    - *Optical fiber interface*
    - *R/W capability*
  - Interface to GPS (need ref clock & 1 pps for timestamp counter resets)
    - *Read link: receive data streams from L2 crates*
    - *Write link: encode clock & data, handles resetting system*



Faster Technology
P6 PCI FPGA Card